II. REMARKS

Claims 1-31 and 33-63 are pending, and claims 1-8, 15-24, 34-36 and 43-52 are allowed. The Applicant's attorney, Bryan Santarelli, has amended claims 3-4, 9, and 37, and has added new dependent claims 60-63. The amendments to claims 3-4 place the language of these claims in conformance with that of claim 1, from which claims 3-4 depend.

The Applicant's attorney thanks the Examiner for participating in a phone interview on 09 August 2005. During the interview, the Examiner confirmed that the indication of allowed and rejected claims on the second page (PTOL-326) of the office action is correct, and that the rejection of claims 1-4 and 8 and the objection to claims 5-7 and 34-36 on pages 3 and 9 of the office action are incorrect. The Examiner also agreed that claims 25-31, 33, and 53-59 are allowable as previously pending, and that claims 9-14 and 37-42 are allowable as amended. But if after considering this response the Examiner does not allow all of the claims, then he is requested to schedule another interview with the Applicant's attorney.

In light of the following, all of the claims are now in condition for allowance, and, therefore, the Applicant's attorney requests the Examiner to withdraw all of the outstanding rejections.

Rejection of Claims 9-14, 25-31, 33, 37-42, and 53-57 Under 35 U.S.C. § 102(b) As Being Anticipated By "VLSI Implementation Of Inverse Discrete Cosine Transformer . . .", Masaki et al.

As discussed below, the Applicants' attorney disagrees with this rejection.

Claim 9

Claim 9 as amended recites a processor operable to combine a first matrix column of first intermediate values with a second matrix column of second intermediate values to generate a portion of a resulting matrix column of resulting values, and to store the

resulting values in more than one memory row to convert the portion of the resulting matrix column into a corresponding portion of a resulting matrix row.

For example, referring, *e.g.*, to pp. 12 and 22-23 and FIGS. 12-18 of the patent application, per equation (13) (p. 12), a computing unit 112 (FIG. 13) of a processor 108 (FIG. 12) computes ½ the sum of even Masaki values de_{00} - de_{03} from a first matrix column (equation (12) of p. 12) and respective odd Masaki values do_{00} - do_{03} from a second matrix column (equation (12)) to generate a portion I'_{00} - I'_{03} of a resulting matrix column of resulting values I'_{00} - I'_{07} (equation (13)). Referring to FIGS. 17 and 18, the computing unit 112 then stores I'_{00} - I'_{03} in respective rows Reg1, Reg4, Reg7, and Reg10 to convert the portion I'_{00} - I'_{03} of the resulting matrix column into a corresponding portion of a resulting matrix row (the portion of the matrix row formed by the rightmost locations of Reg1, Reg4, Reg7, and Reg10). That is, storing I'_{00} - I'_{03} in respective rows Reg1, Reg4, Reg7, and Reg10, and storing the other I' values in a corresponding manner, effectively transposes the I' matrix generated per equation (13) for use in equation (12) (in place of the D values) without executing a separate transpose instruction.

In contrast, Masaki does not disclose storing a portion of a matrix column of resulting values in more than one memory row. Referring, *e.g.*, to FIG. 5, Masaki's 1-D IDCT circuit generates first and second portions $x_3 - x_0$ and $x_4 - x_7$ of a resulting matrix column of resulting intermediate inverse-transform values x_0 - x_7, which respectively correspond to I'_{00} - I'_{07} of equation (13) of the patent application (see the previous paragraph). Then, Masaki's IDCT circuit (FIG. 5) loads $x_3 - x_0$ and $x_4 - x_7$ into the top row of the memory of FIG. 6(a), and inverts the order of the first portion ($x_3 - x_0 \rightarrow x_0 - x_3$) while loading such that the top row of the memory in FIG. 6(a) contains x_0 - x_7 in the positions 1, 2, 3, 4, 4, 3, 2, 1, respectively. That is, unlike the processor recited in claim 9, Masaki's IDCT circuit stores the first portion $x_0 - x_3$ of the resulting matrix column x_0 - x_7 in a single memory row, not in more than one memory row. And also unlike the processor recited in claim 9, Masaki's IDCT circuit stores the second portion x_4 - x_7 of the resulting matrix column x_0 - x_7 in a single memory row, not in more than one memory row.

Consequently, unlike the processor recited in claim 9, Masaki must execute a separate transpose instruction per FIG. 6(b) to transpose the *x* matrix.

Claims 10-14, 58, and 60-63

These claims are patentable by virtue of their dependency from claim 9.

Claim 25

Claim 25 recites a processor operable to store pixel values that respectively occupy every other position of a row in a first continuous section of a register and to store the pixel values that respectively occupy remaining positions of the row in a second continuous section of the register.

For example, referring to FIGS. 3, 13 and 16 and equation (12) (p. 12) of the patent application, a computing unit 112 (FIG. 13) of a processor 108 (FIG. 12) receives discrete cosine transform (pixel) values $D_{00} - D_{07}$ (FIG. 3) that each occupy a respective position within a row of pixel values. Because equation (12) requires that these values be rearranged into even and odd portions D_{00}, D_{02}, D_{04}, D_{06} and D_{01}, D_{03}, D_{05}, D_{07} of a matrix column, the unit 112 executes an inverse zig-zag operation that stores in the left half (a first continuous section) of a register 136a (FIG. 16) the pixel values (*e.g,* D_{00}, D_{02}, D_{04}, D_{06}) that occupy every other position of the row, and stores in the right half (second continuous section) of the register 136a the pixel values (*e.g.,* D_{01}, D_{03}, D_{05}, D_{07}) that occupy the remaining positions of the row.

In contrast, Masaki does not disclose storing pixel values that respectively occupy every other position of a row in a first continuous section of a register, or storing the pixel values that respectively occupy remaining positions of the row in a second continuous section of the register. Referring, *e.g.,* to FIG. 5, Masaki's 1-D IDCT circuit generates first and second groups $x_3 - x_0$ and $x_4 - x_7$ of intermediate inverse-transform values, and inverts the order of the first group ($x_3 - x_0 \rightarrow x_0 - x_3$) such that the top row of the memory in FIG. 6(a) contains x_0 - x_7 in the positions 1, 2, 3, 4, 4, 3, 2, 1 respectively. But inverting the

order of first group $x_3 - x_0$ is not the same as the claimed technique, which would yield x_3, x_1, x_4, x_6, x_2, x_0, x_5, x_7 in the top row of Masaki's memory. Furthermore, Masaki does not disclose how he stores the DCT values $X_1 - X_7$ for manipulation per Masaki's equation (7).

Claims 26-29

These claims are patentable by virtue of their dependencies from claim 25.

Claim 30

As discussed with the Examiner on 09 August 2005, claim 30 is a method claim that corresponds to, and thus is similar to, the image-decoder claim 1. Therefore, claim 30 is patentable for reasons similar to those previously recited in support of the patentability of claim 1.

Claims 31 and 33

These claims are patentable by virtue of their dependency from claim 30.

Claim 37

As discussed with the Examiner on 09 August 2005, claim 37 is a method claim that corresponds to, and thus is similar to, the image-decoder claim 9. Therefore, claim 37 as amended is patentable for reasons similar to those recited above in support of the patentability of claim 9.

Claims 38-42 and 59

These claims are patentable by virtue of their dependencies from claim 37.

Claim 53

As discussed with the Examiner on 09 August 2005, claim 53 is a method claim that corresponds to, and thus is similar to, the image-decoder claim 25. Therefore, claim 53 is patentable for reasons similar to those recited above in support of the patentability of claim 25.

Claim 54 - 57

These claims are patentable by virtue of their dependencies on claim 53.

Conclusion

In light of the foregoing and in addition to the allowed claims 1-8, 15-24, 34-36, and 43-52, claims 10-14, 25-31, 33, 38-42, and 53-59 as previously pending, claims 9 and 37 as amended, and new claims 60-63 are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

DATED this 10th day of August, 2005.

Respectfully Submitted,

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